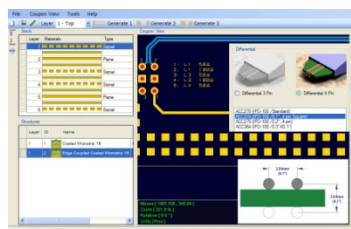
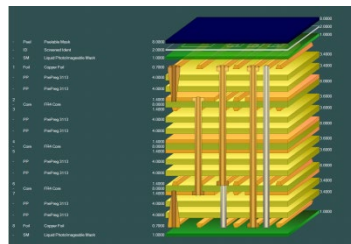
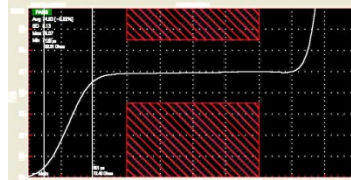
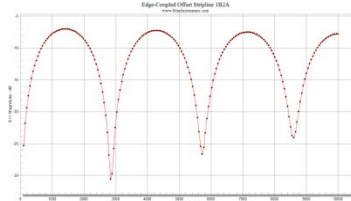
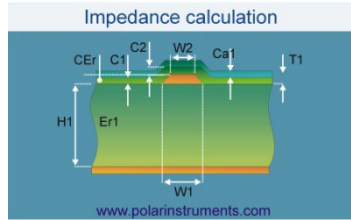


CITS880s & TRC Plus 2022 Preview

Accurate characteristic impedance measurement for fine line traces



Edge-Coupled Offset Stripline 1B2A

Substrate 1 Height: H1 = 72.90

Substrate 1 Dielectric: Er1 = 3.2000

Substrate 2 Height: H2 = 71.88

Substrate 2 Dielectric: Er2 = 3.4500

Substrate 3 Height: H3 = 71.88

Substrate 3 Dielectric: Er3 = 3.6000

Lower Trace Width: W1 = 82.04

Upper Trace Width: W2 = 70.10

Trace Separation: S1 = 148.08

Trace Thickness: T1 = 16.00

Notes: (First 5 lines will print)

Add your comments here

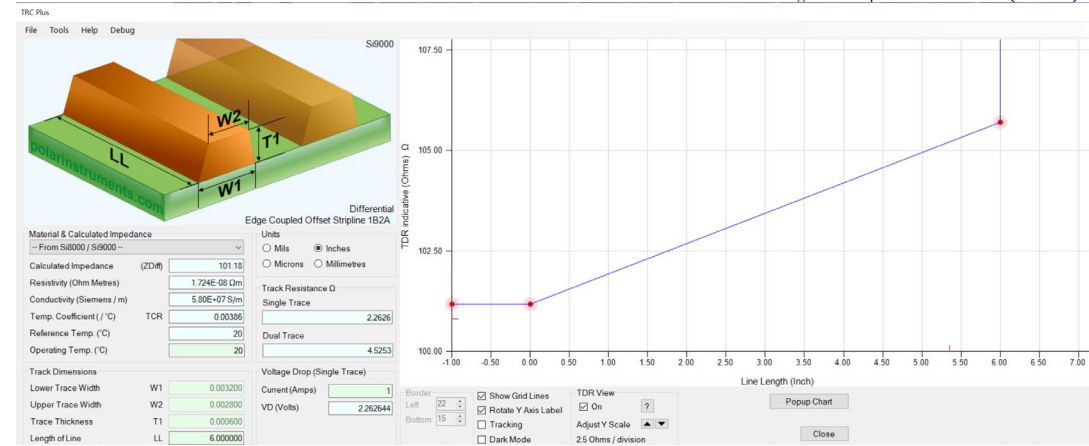
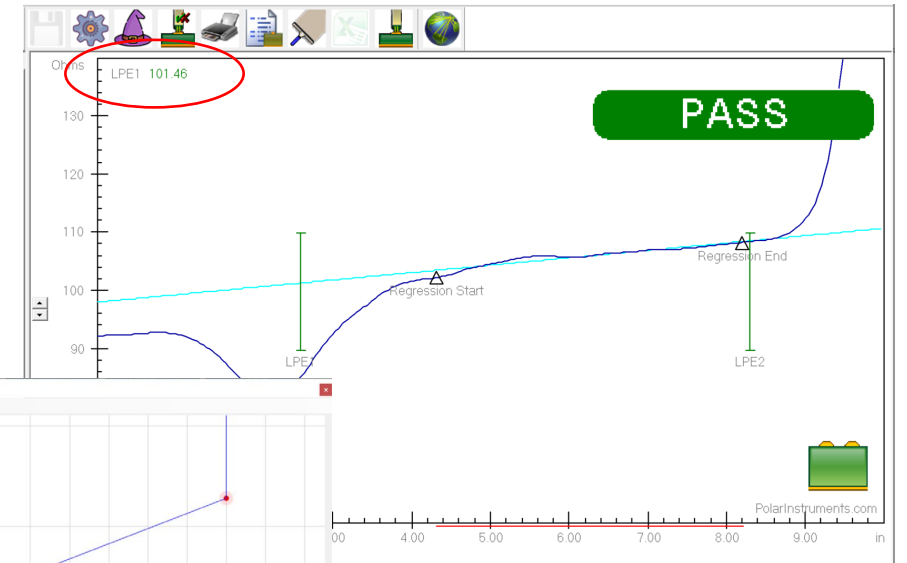
Interface Style

☒ Standard

☐ Extended

Differential Impedance

Zdiff = 101.18



Introducing CITS880s & TRC Plus 2022

Welcome to a preview of CITS880s & TRC Plus 2022.

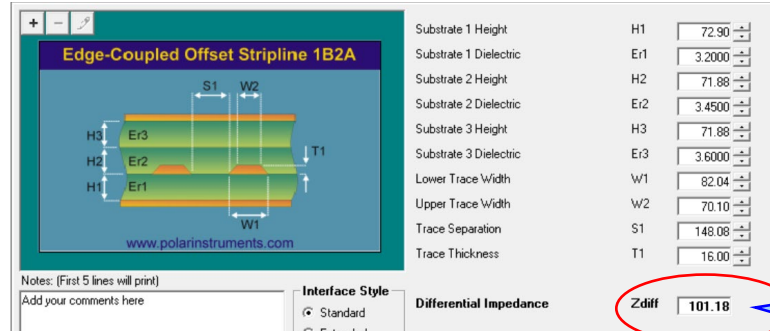
We have introduced a number of new features that have been driven through the need to more accurately measure the characteristic impedance on fine line PCB traces.

If you would like to have a web-based demonstration please contact your local Polar office, details are shown on the last slide of this presentation.

Please note: TRC Plus is a bolt on option for the Si8000m and Si9000e impedance field solvers

CITS880s and TRC Plus v22.XX (February 2022)

Enhancements targeted at improvements in impedance correlation on fine line PCB traces

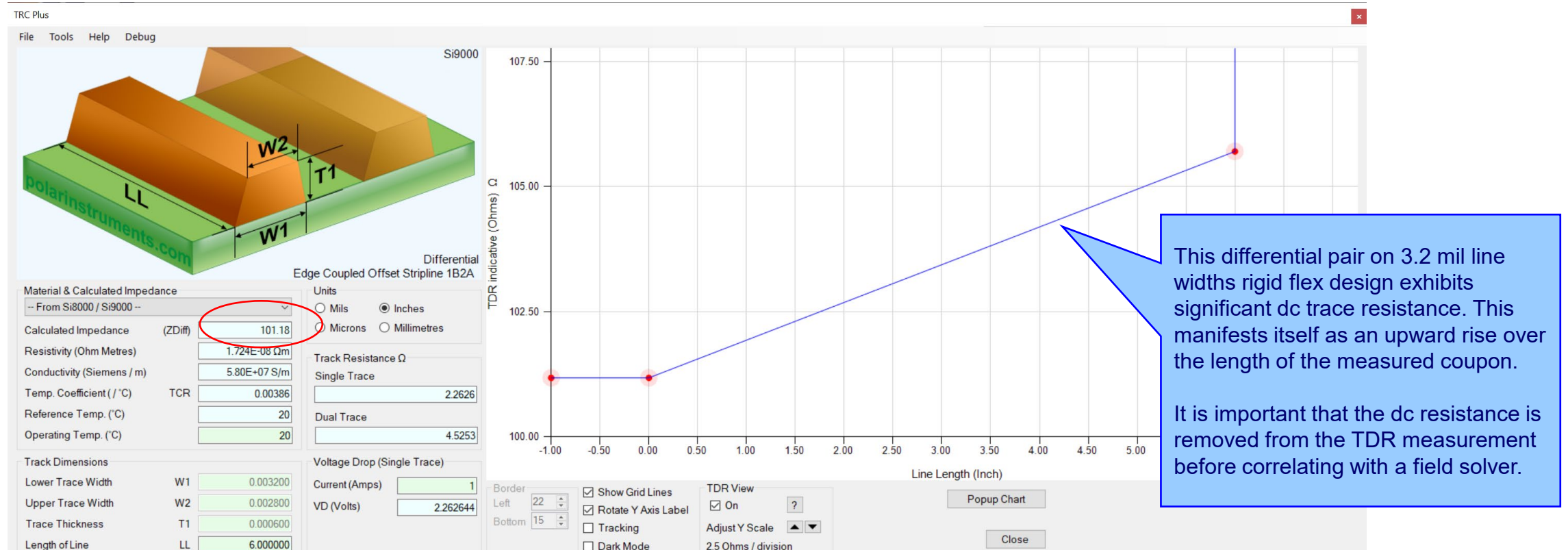


The goal of designer & fabricator is:

1. To ensure the most accurate correlation between the design and fabricated impedance
2. CITS880s and TRC Plus are enhanced to simplify this from both the design & fabrication perspectives.

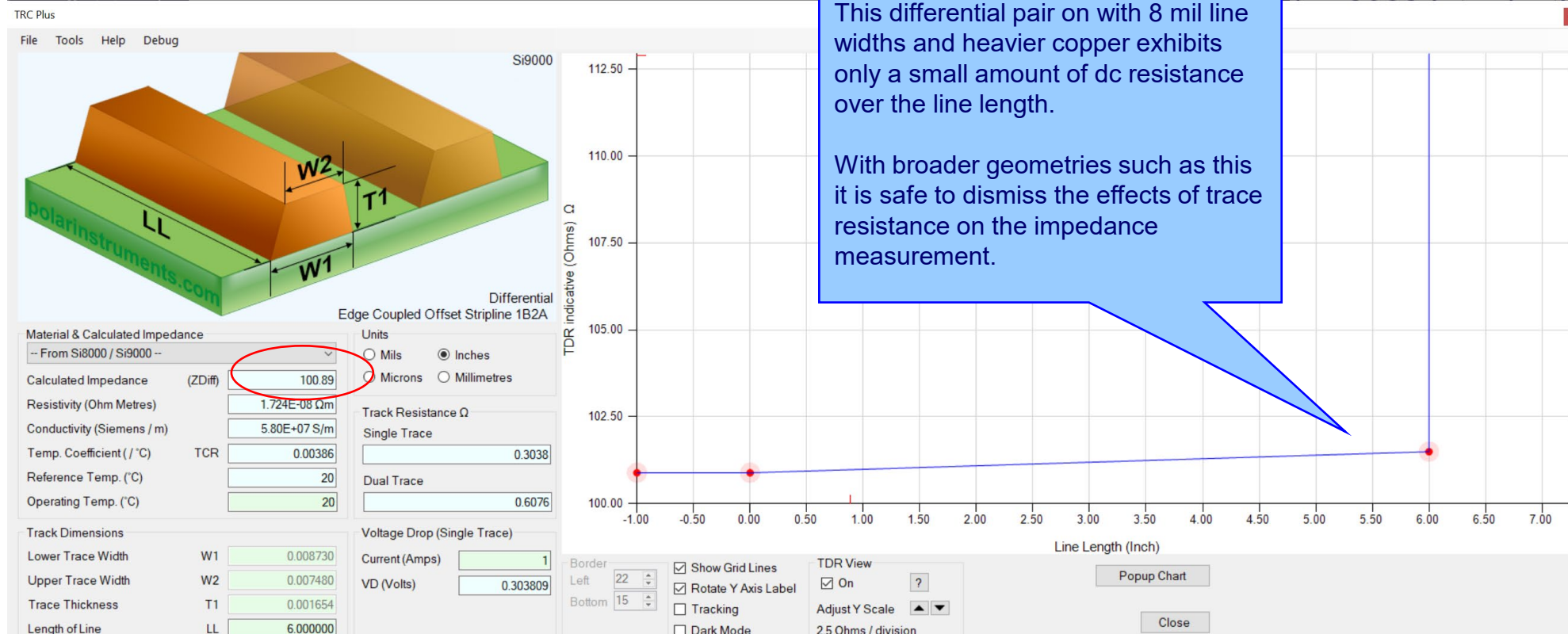
The 2022 enhancements in CITS880s and TRC Plus aid this process for fine line PCBs and thin flexible and rigid flex constructions

Fine line traces – the impact of trace resistance on TDR measurement



“TDR View” now graphically gives you an idealised TDR waveform including the predicted impact of trace resistance.

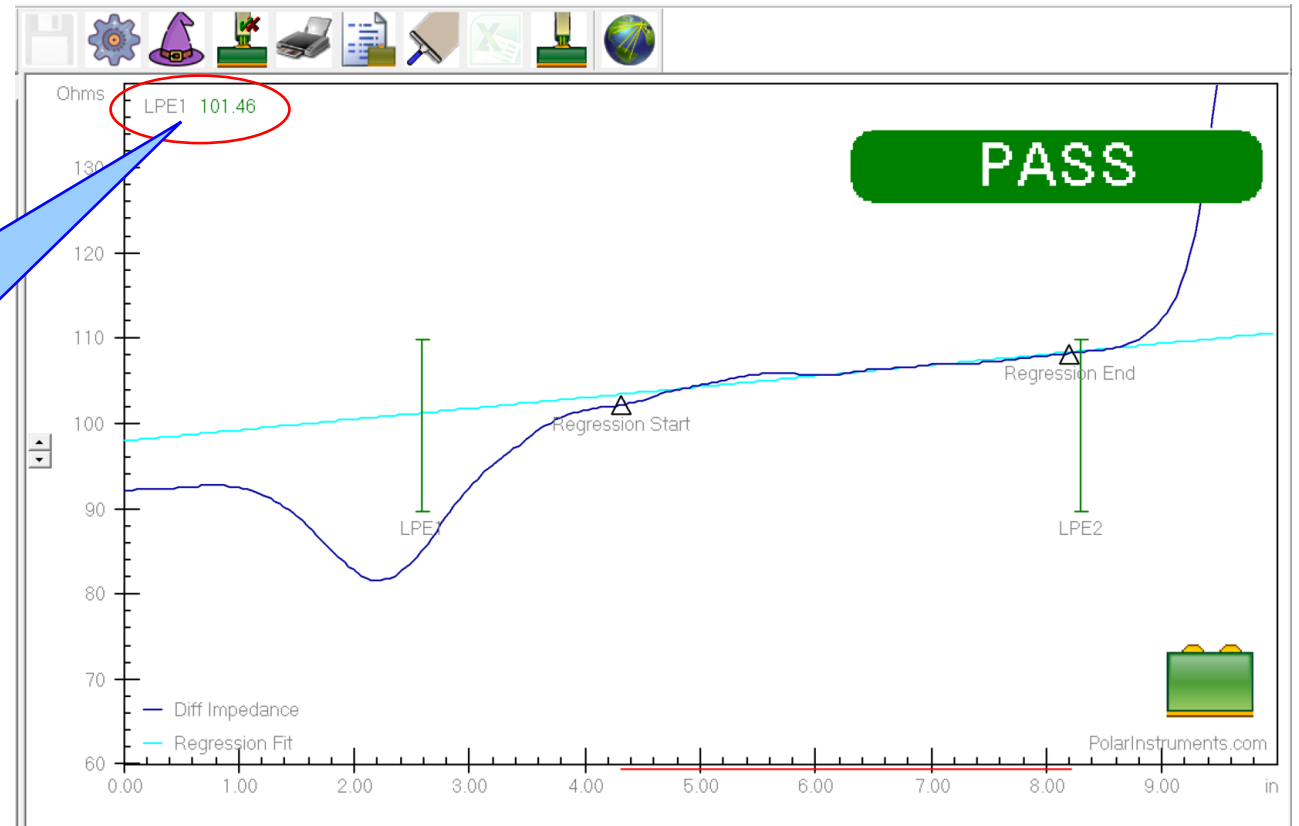
Wider traces – the impact of dc resistance on TDR measurement may be ignored



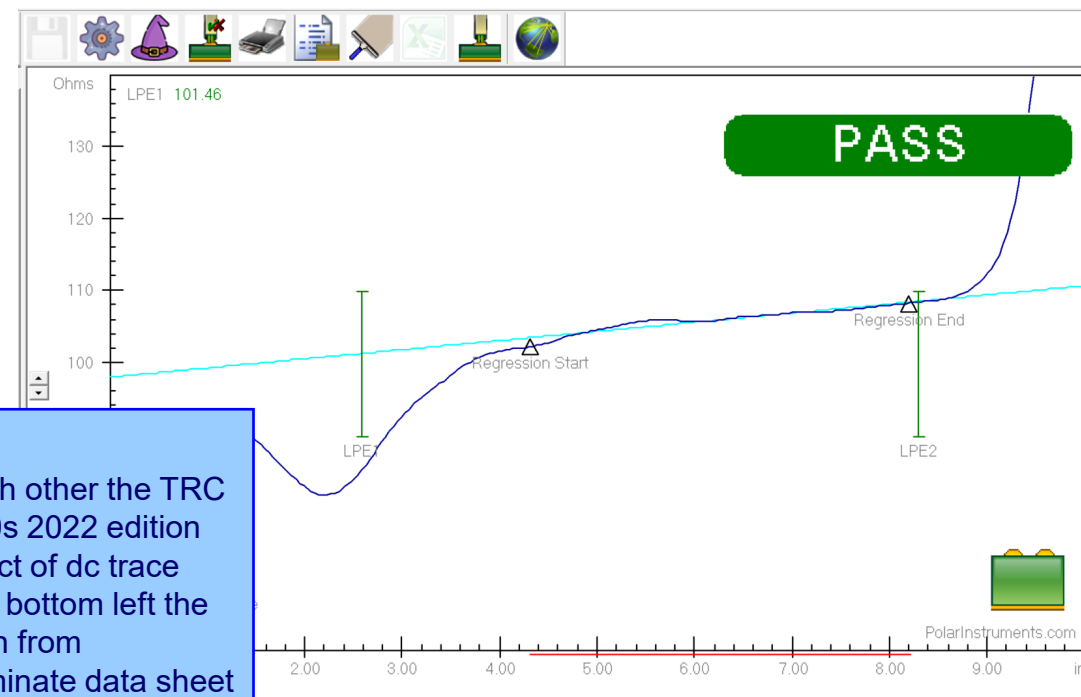
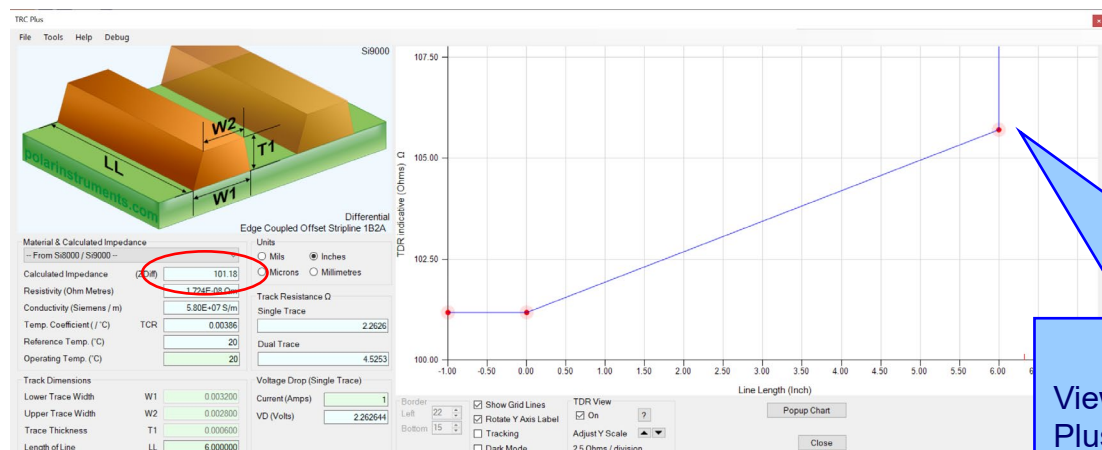
CITS880s – a cleaner interface for fine line measurement tools

Launch point extrapolation and dc resistance compensation are two valid methods for de embedding the dc resistance from a TDR trace.

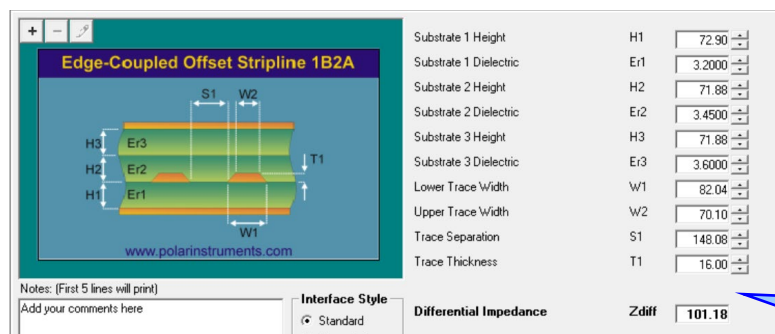
CITS880s introduces a simplified display clearly indicating the line fit used to extrapolate the characteristic impedance measured at the launch of the trace.



Fine line traces – the impact of trace resistance on TDR measurement



Viewed alongside each other the TRC Plus and the CITS880s 2022 edition clearly show the impact of dc trace resistance. And at the bottom left the solver prediction taken from microsections and laminate data sheet figures for dielectric constant show excellent correlation.



The solver prediction taken from microsections and laminate data sheet figures for dielectric constant show excellent correlation.

CITS880s – a cleaner interface for fine line measurement tools

Test Setup Editor - Administrator Access (Full)

Description:

Probe & Channel Select

- ☐ Single-Ended Test
- ☒ Differential Test
- ☐ Groundless Differential Test

Ch1 & Ch2

OK Cancel Defaults

Edit Structure

Edge-Coupled Surface Microstrip 1B

Probe Length: 4.70 Inches

LPE Regression Start: 4.32 Inches

LPE Regression End: 8.19 Inches

Display Width: Default Inches

Autoscale

Tolerance

- ☐ Intermediate
- ☒ Locked
- ☒ %
- ☐ Ohms

Plus: 10.00

% (10.00 Ohms)

Enable Max-Min

Unbalance Warning: 15.00 %

Enable

Group Name

Maximum Spread Ohms

Fine Line Compensation

DC Resistance Comp.

- ☒ Default
- ☐ User
- ☐ Normalized

Launch Point Extrapolation

Enable	Ohms	Distance
<input type="checkbox"/>	100.00	2.58 Inches
<input checked="" type="checkbox"/> Pt2	100.00	8.30 Inches

Test Method

- ☐ Average
- ☐ Absolute
- ☐ Envelope
- ☒ LPE

File Timestamp :- Monday, February 07, 2022 18:39:24

Fine line test methods are grouped in a simplified test editor interface. (Some OEMs prefer LPE – others DC resistance compensation) – both are valid.

CITS880s 2022 introduces a simplified edit menu with a specific LPE test method. The new editor combined with the simplified CITS display for LPE make for easy to set up and accurate impedance measurement on fine line traces

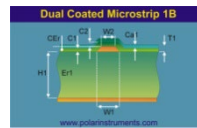
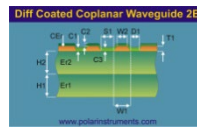
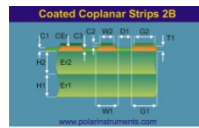
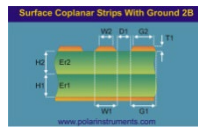
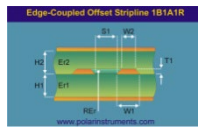
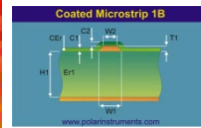
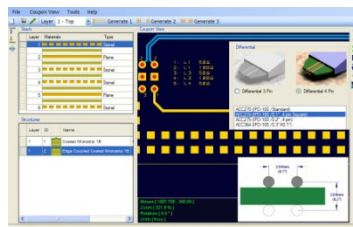
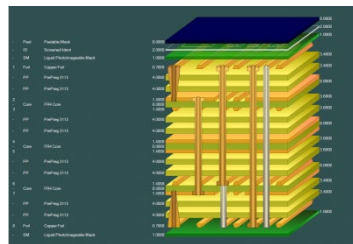
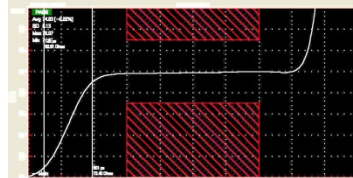
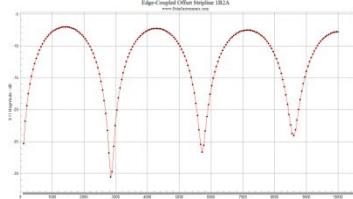
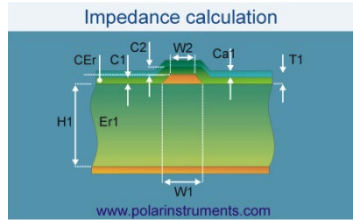
What if I don't take into account the effect of dc resistance on TDR impedance measurement?

If you ignore the dc resistance effect on fine line traces you will note the TDR reading is high compared with predictions. This may lead you to conclude the data sheet value for ϵ_r is incorrect, maybe even going onto “goal seeking” an ϵ_r value that will allow you to meet the impedance with a revised geometry.

Laminate suppliers provide accurate measurements for ϵ_r – and in Polars experience de embedding the dc resistance allows you to better correlate results without artificially adjusting ϵ_r values/

If you would like to have a web-based demonstration please contact your local Polar office, details are shown on the last slide of this presentation.

Please note: TRC Plus is an option for both the Si8000m and Si9000e impedance field solvers



Thank you for viewing this CITS880s & TRC Plus 2022 preview. If you have questions we would be delighted to help you.

Edge-Coupled Offset Stripline 1B2A

Substrate 1 Height: H1 = 72.90

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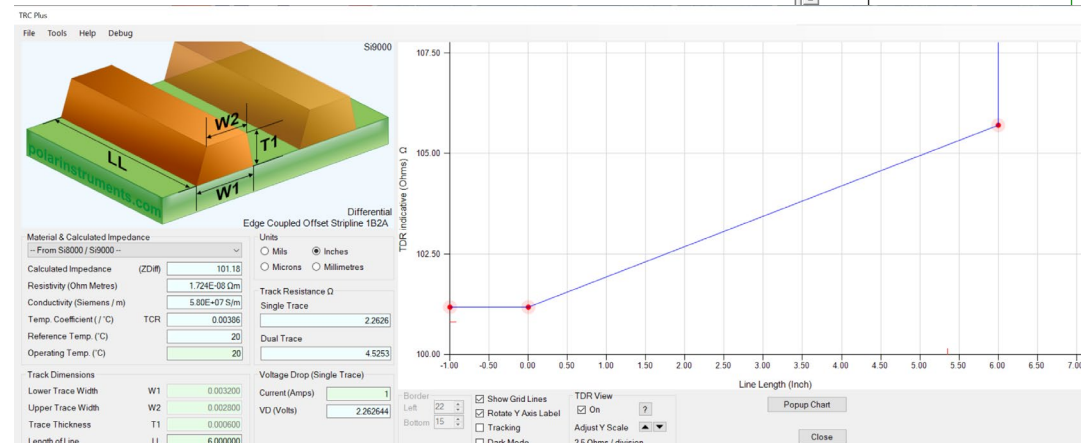
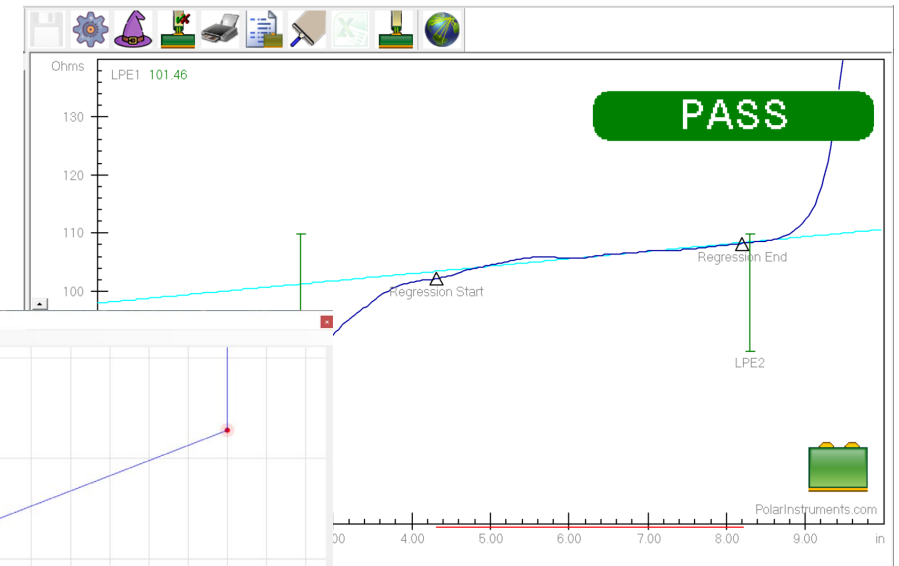
Add your comments here

Interface Style

Standard

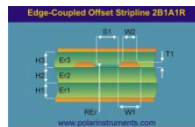
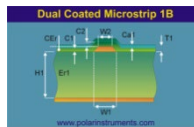
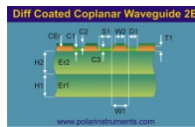
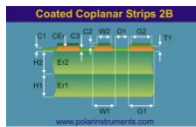
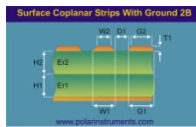
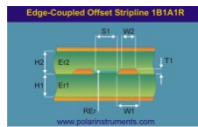
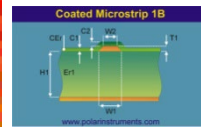
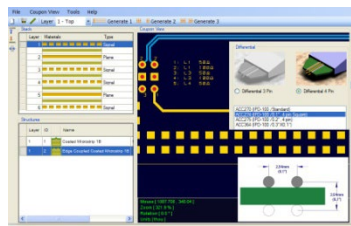
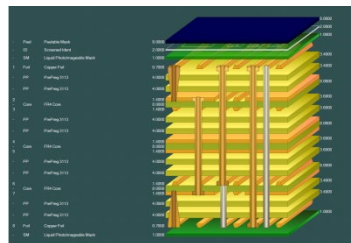
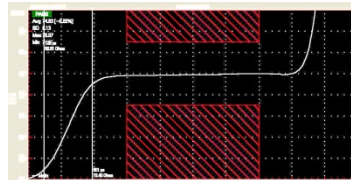
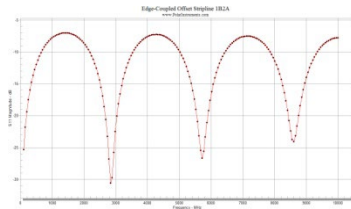
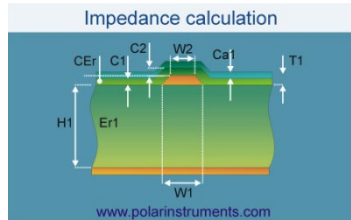
Differential Impedance

Zdiff = 101.18



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